FUNCTIONAL DESCRIPTION OF THE PROFILE ANALOG BOARD

(Refer to the six page schematic for reference details)

The following document has been written with the purpose of describing the circuitry on the Profile Analog Board in detail. It is not meant to be a troubleshooting guide, but is aimed at informing the technician of the different circuits and operating parameters of the board. This document should be used with the Profile Analog Board Tester, Apple Part # 890-0184, in testing and repairing any problem on the board.

In the event that it is desired to troubleshoot the board onboard the Profile unit itself, the board may be accessed using the following method:

Turn the Profile off and let it sit for a minute until the drive stops rotating. Access the Profile Analog board by turning the Profile over on its top, providing the top cover is on the unit. Remove the metal cover under the cabinet which accesses the Analog board. Power the drive back up and refer to the schematic for the test points and waveforms. No harm can come to the drive while it is running in this position, but random data errors will probably occur. Make sure that the drive cannot fall over or receive any sharp jolt or shock as this will damage the HDA media.

223 direct.

0 & 1 - Spare or 0 & 1

The connector J2 on the left connects the Analog board to the Controller board. The signals coming into the board are the write data (NRZWDTA), the 10mhz write clock (2F), the write precompensation and current control signal (PCOMP-LOCUR), and the write gate signal (WTGT). Outputs to the Controller board are the TRK 0 detection and Index pulse signals coming from the HDA assembly. Power and ground inputs to the board are also shown for reference.

The track 0 signal indicates when the head stepper motor assembly is at track 0 or the outer track location, while the index pulse occurs once per drive revolution. The index pulse can be monitored at test point TP-9 and used as an oscilloscope trigger for viewing the track analog data at test point TP-1.

The +/- 0A and +/- 0B stepper motor control phases pass through the board and are routed to the HDA stepper motor at connector J7.

The Track 0 signal is obtained from the photosensor mounted on the HDA stepper motor. The sensor is tripped by the rotating arm assembly on the motor shaft when the head array is at the track 0 position, and the sensor output comes in the board at connector J6. The signal is detected and amplified by device UC30 and passed to the Controller board at J2 pin 2.

The Index signal comes from the photosensor mounted under the HDA. The sensor is tripped by a small metal tab fastened to the bottom plastic cover of the drive spin motor and comes in the board at connector J8. The signal is detected and amplified by device UC30 and passed to the Controller board at J2 pin 4.

The write encoding and precompensation circuitry consists of devices UC27, 28, 29, and 30. The 10mhz write clock is divided by UC2 to create a 5mhz clock (1F) for VCO reset control purposes. The data and control signals are decoded by the PAL logic array UC28, and DLY 2 provides delay references of 10 and 20nsec for data signal precompensation.

This is done to compensate for the magnetic fluxes on the disk media trying to repel each other because of their polarity differences. If this happens, the flux reversals on the media will all have more or less the same distance between them, resulting in a sine wave pattern on the disk with no 1F or 2F signal component margin between flux reversals.

The signal outputs of the PAL indicate Early, On Time, or Late data occurances as detected in the PAL data register. These are generated by comparing the data bit pattern and defining the three potential transition points for every flux reversal with the write timing. These signals then shift the write data signal by selecting the proper amount of delay (usually 20 nsec) to over-write any potential bit shift on the media surface. This precompensates the data on the disk surface, allowing a higher bit density without loss of resolution.

On this page are the write amplifier, write current control, head select, and read detection circuitry. The write data (WXS) is gated through UC2 into the write current driver array UC1 (MPQ6700) and UC31 (MPQ2907). The data through UC2 will be blocked if the WRTSM' write sector mark signal is true, as this is used to write blank areas on the track for disk sector formatting identification.

The current level of the final driver transistor array is set by a voltage reference developed across zener CR1. This diode has a value of 1.2 to 1.25 VDC, which sets the drive level of UC1 to 24ma of write current (48ma peak-to-peak).

This level is used to write tracks 0 through 128, while tracks 129 to 152 use less current because of the thinner media coating and smaller disk radial area per bit on the inner tracks. Remember that the drive spin is a constant speed, and the head covers more area on an outer track than it does an inner track during the same time period. In addition, the media surface coating on the disk is thinner towards the center. The smaller available area requires less current to effectively write the media than the larger.

To set the lower current value, the PCOMP-LOCUR' (Precompensation- Low Current) signal goes active, causing UC3 to "steal" 5ma from the write current value through the 1.78kohm resistor R10. This results in a lower head write current level of 19ma (38ma peak-to-peak) for the inner tracks.

The write current passes through diodes CR4 and CR13 to four connector pins ABCD, and from there directly to the heads. If desired, a pin to pin wire loop can be used at pins AB or CD to monitor the actual write current with a current probe, as the pins are shunted with 22 ohm resistors to the head matrix.

Signals HS-1 and HS-0 are decoded by 1 of 4 decoder UC4. The output selects one of the four heads for either reading or writing by correctly biasing the center tap of the head coil. The other heads are held in an off condition allowing only one head to be selected at a time.

The POWEROK signal is a monitor function of the power supply and instantly terminates any write signal if the main power to the Profile unit is lost. The POWEROK line is dropped low by the power supply if the incoming AC is lost, causing the voltage drop across R16 to turn on UC13. This cuts off UC1 while there is still power out of the supply maintaining the system electronics. The POWEROK signal also holds the stepper motor, Z8 controller, and write amplifiers off for a brief moment after initial power on. This delay action can be seen by the READY lamp on the front panel lighting for 1 to 1 & 1/2 seconds when Profile power is first turned on.

The WRTSM' signal is used to "write" (actually erase) the track sector marks. The Profile uses 16 blank sector marks per track radially aligned on the disk, and this signal inhibits any write action to the head during the formatting of the these areas on the disk.

The sector marks are erased as 20usec long blank spaces and the disk read logic needs a minimum of 10usec to identify the mark. If any sector mark on a track is written over, the data in that sector is effectively destroyed and cannot be used.

For read operation the forward biased diode matrix detects the differential analog transitions (-X and -Y) of the selected head. The other heads are biased so that there is no current flow in the coil, preventing any signal detection. The analog signal transitions are extremely small and attempting to view them in this diode network is impossible.

The -X and -Y analog signals enter the ECL 10114 preamplifiers, which are power supply isolated by RG1 for noise immunity. The 10114 was selected because of its excellent input geometry with very little noise. The signals then pass through a low pass filter which is set for 7.5Mhz, or 3 times the maximum read signal frequency of 2.5Mhz (2F).

This filter attenuates the major error element of the detected signal, which is the third harmonic of the flux reversal. If viewed on a scope, this is the "knee" part of the waveform transition midway between signal peaks. The signal then enters a 592 video amplifier UC6, which acts as the AGC (Automatic Gain Control) integrator and controller.

The AGC level is developed by device Q3, a VCR2N junction whose bias level is controlled by UC8, a 353 AGC detector and amplifier. The AGC controlled output of the 592 passes through an emitter follower and buffer network UC7 and is available for monitoring purposes at test points TP1 and TP2 at the bottom of the page. These are differential signals and can be shown individually or compared with each other.

The signal levels at these test points are still analog in form and should be around 1.5 to 2 volts peak-to-peak. Anything outside of these levels is indicative of a bad AGC network and renders the data unreadable to the system. If the AGC is lost, the Profile cannot perform the initial scan function after power up.

If this should happen, suspect anything in this network. However, remember that the signals into the circuit are far too small to be monitored directly. The best way to troubleshoot anything in this area is to swap out the ICs in the circuit. Troubleshooting to a bad component other than an IC is almost impossible and the board may have to be scrapped out if any other component is at fault.

To the right of the UC8 pin 7 is a jumper used to set the AGC at a fixed level referenced to -12VDC. This is done only in board manufacture test and the jumper should never be found in the field. Remove it if installed.

The AGC controlled analog signals enter two 10116 ECL schmitt level circuits (UC9) which make up the zero crossing detector. If any signal dropout occurs because of poor AGC, it will be detected by this circuit and interpreted as data.

The upper portion of the circuit sets the gain for a minimum amplitude symmetrical signal level. The lower circuit has a delay line in parallel which acts as a 1/4 wavelength delay line through the sum and cancel effect on the signal. In addition, the delay line acts as a good low pass filter to eliminate "hash". The output of the OR gate UC10 is the detected signal pulse. This is allowed to happen only during the "signal allowed" period set by the delay circuit.

The detected signal is then gated through UC11 which outputs a low going pulse for every signal that is detected by the zero crossing detector circuit. The output of UC11 is developed by an RC network consisting of C20, R65, and R66, which forms a 50nsec pulse for every flip-flop transition of UC11. If the pulse width is less than 40nsec, capacitor C20 should be replaced to increase the time factor and corresponding pulse width.

As previously outlined, Profile uses blank areas on the track for sector identification. These marks indicate the 16 individual track sectors and are placed on the track when it is initially formatted. If any sector mark is over-written or lost, that one sector cannot be read by the system and the data within it is lost.

Another schmitt trigger device (UC13) coupled with a slow response time RC circuit is used to detect these blank marks and will not detect any "no signal" period less than 10usec long. The input develops the signal across CR18, CR19, and CR20 with the RC circuit of C23 and R74 delaying the response of one side of UC13.

This means that sector cannot be detected if any noise or off track data has overwritten the blank disk area to the point where it is less than 10usec long. The sectors are written in 20usec period during formatting, so some degradation can occur before the sector is completely lost.

The AM HOLD or address mark hold is a function of the Write Sector Mark and Write Gate signals on page 2. It is used to clamp the circuit during write operations, which prevents the output from indexing any data to the controller card.

On this page are the VCO (Voltage Controlled Oscillator) phase comparator control and data output circuits.

The read gate RDGT provides the control element for the circuit. The VCO is reset during any "no read" condition by the 1F 5Mhz signal. This allows the VCO to be triggered almost instantaneously by the RDGT signal instead of recovering from an extreme compliance condition. The circuit at the top of the page sets the time constant of the reset signal (usually a few microseconds).

When the read gate goes active it triggers the VCO. The circuit then acts to lock the leading edge of the VCO pulse to the leading edge of the 50nsec signal data pulse. This is done by phase comparing the data pulse with the VCO pulse and generating a corresponding +/- INC or +/- DEC control signal. This pulse goes to the charge pump on page 6 which controls the VCO operating frequency. It takes about 20 read data pulses to properly control the VCO as the pulse train consists data pulses at different intervals due to MFM criteria.

The net effect of the VCO control is to compensate for any difference between the read circuit timing and the speed of the disk. Any speed difference creates an error in the data decoding as the data has to occur at 200nsec cycle periods. The VCO compensates for this, allowing a motor speed deviation of up to 3%.

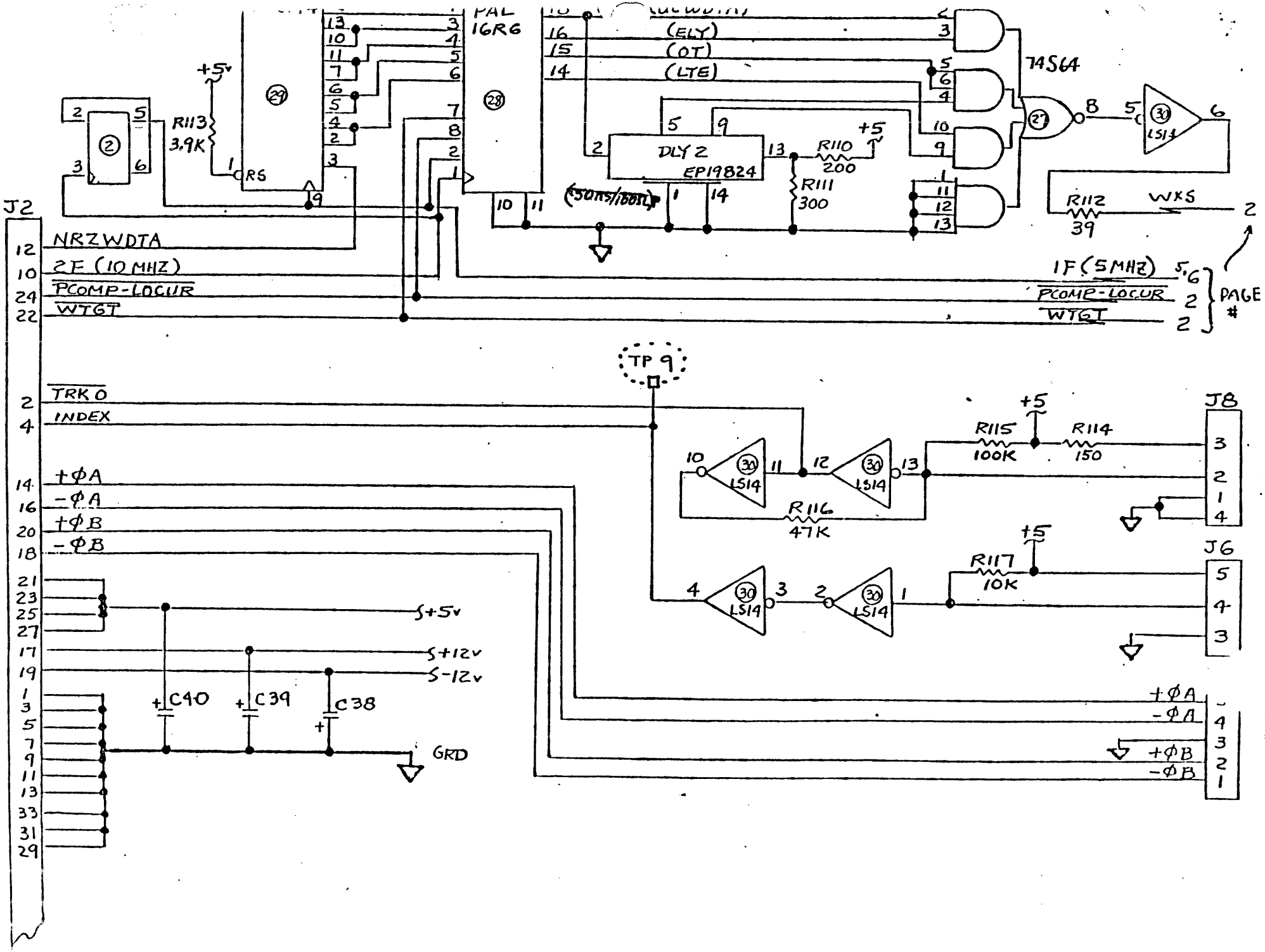
The circuit does this by acting as a "lock", which keeps the data referenced to the center of the VCO pulse "window". The lock lines up the data pulse in the center of the window for stability and proper detection. The VCO output and the data pulse can be monitored at (TP6 and TP7, respectively) to verify the leading edge of both signals occurring simultaneously.

The last portion of the circuit is the ECL to TTL level transition network at the bottom of the page. The detected NRZ data and clock signals are fed to the Controller board through connector J2.

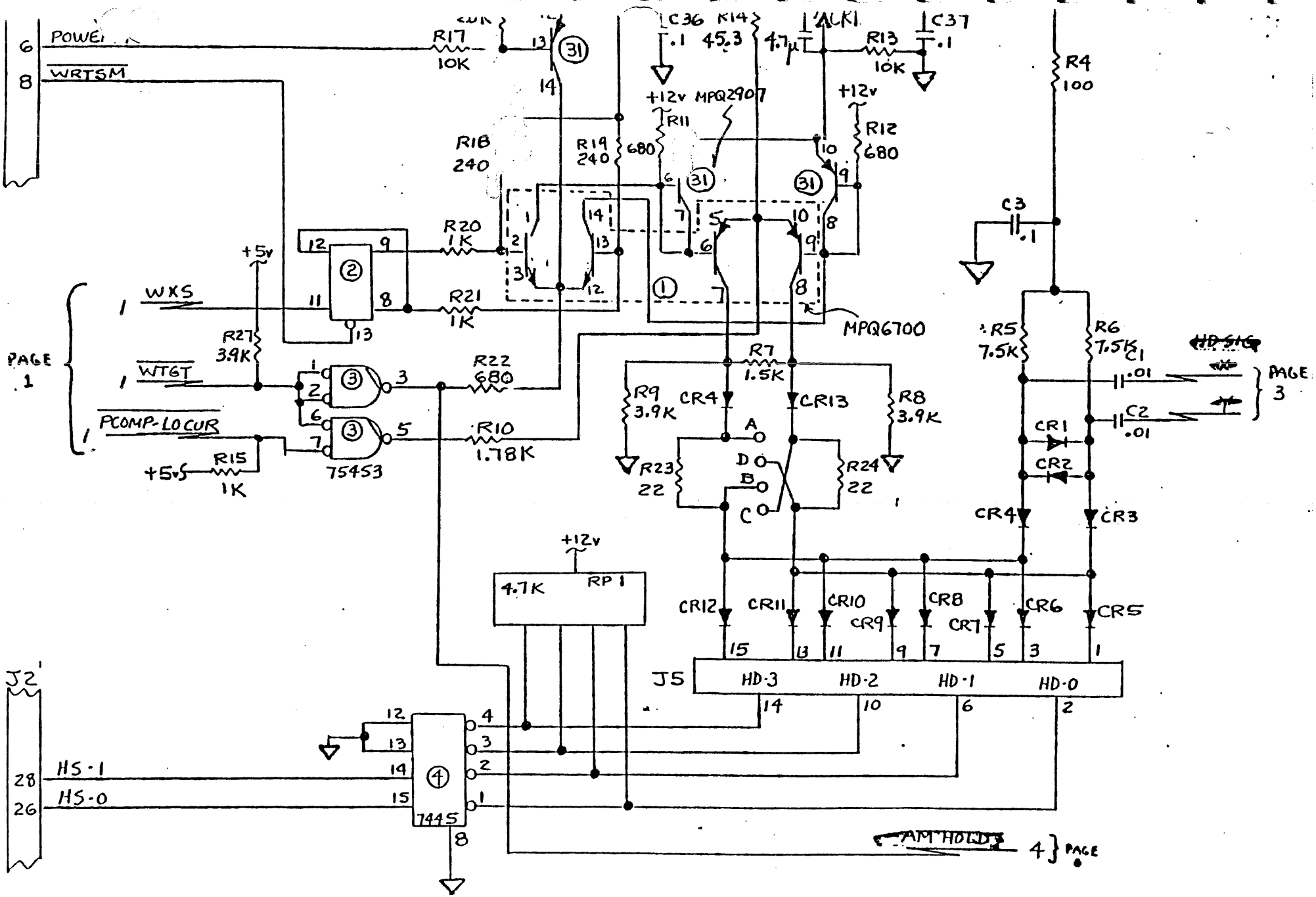
On this page is the VCO circuit itself. The main portion of the circuit is the "charge pump" formed with UC24 and the network around it. The voltage level of the circuit is controlled by the INC -/+ and DEC -/+ signals from page 5. The input of the network acts as a "sample and hold" circuit, setting the current level of the ouput transistors.

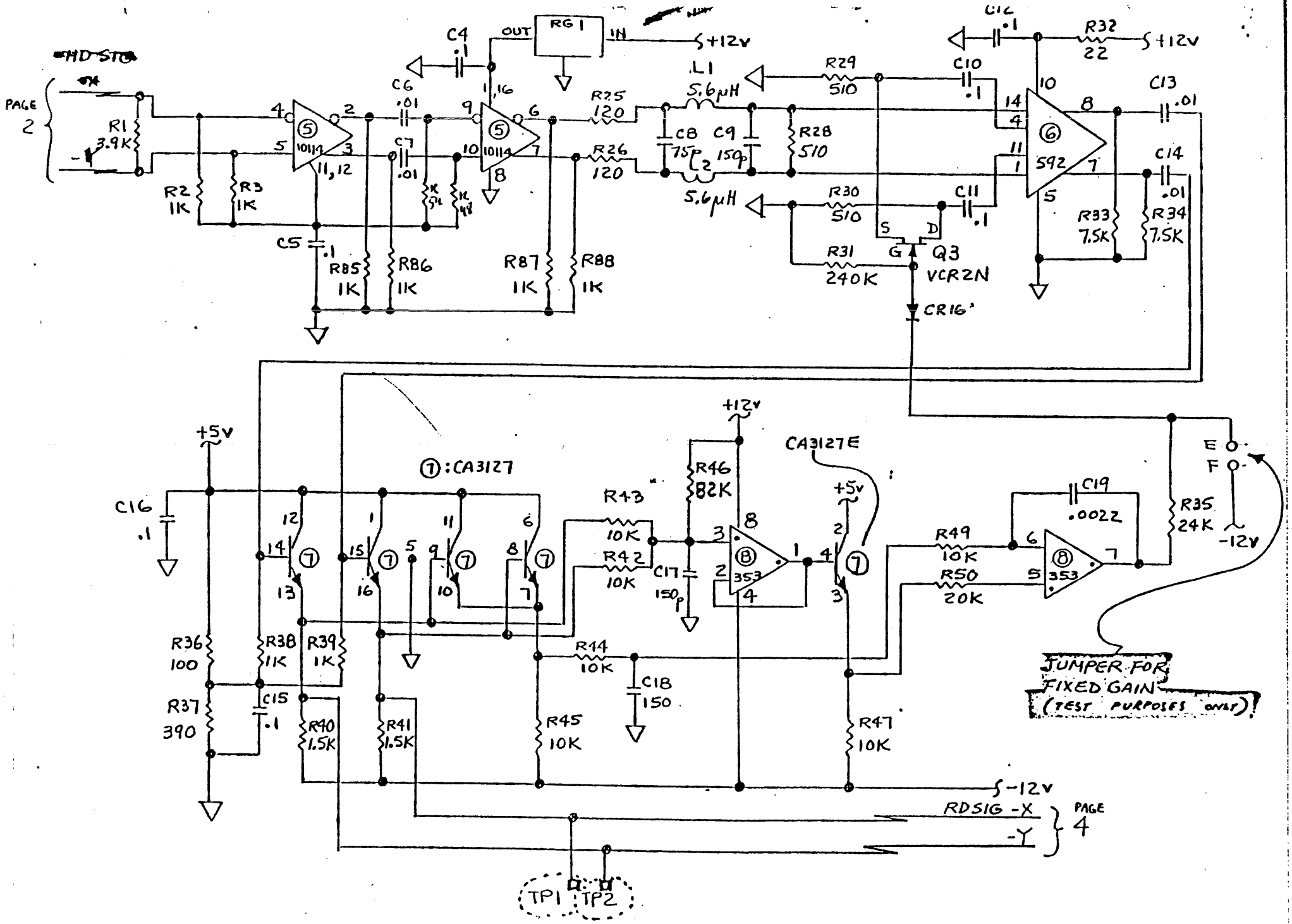
The output passes through a low pass RC filter to a buffer amp UC25. This serves to buffer the current that sets the voltage control level at the MV104 varactor, controlling the VCO frequency. The output of the charge pump can be monitored at TP8.

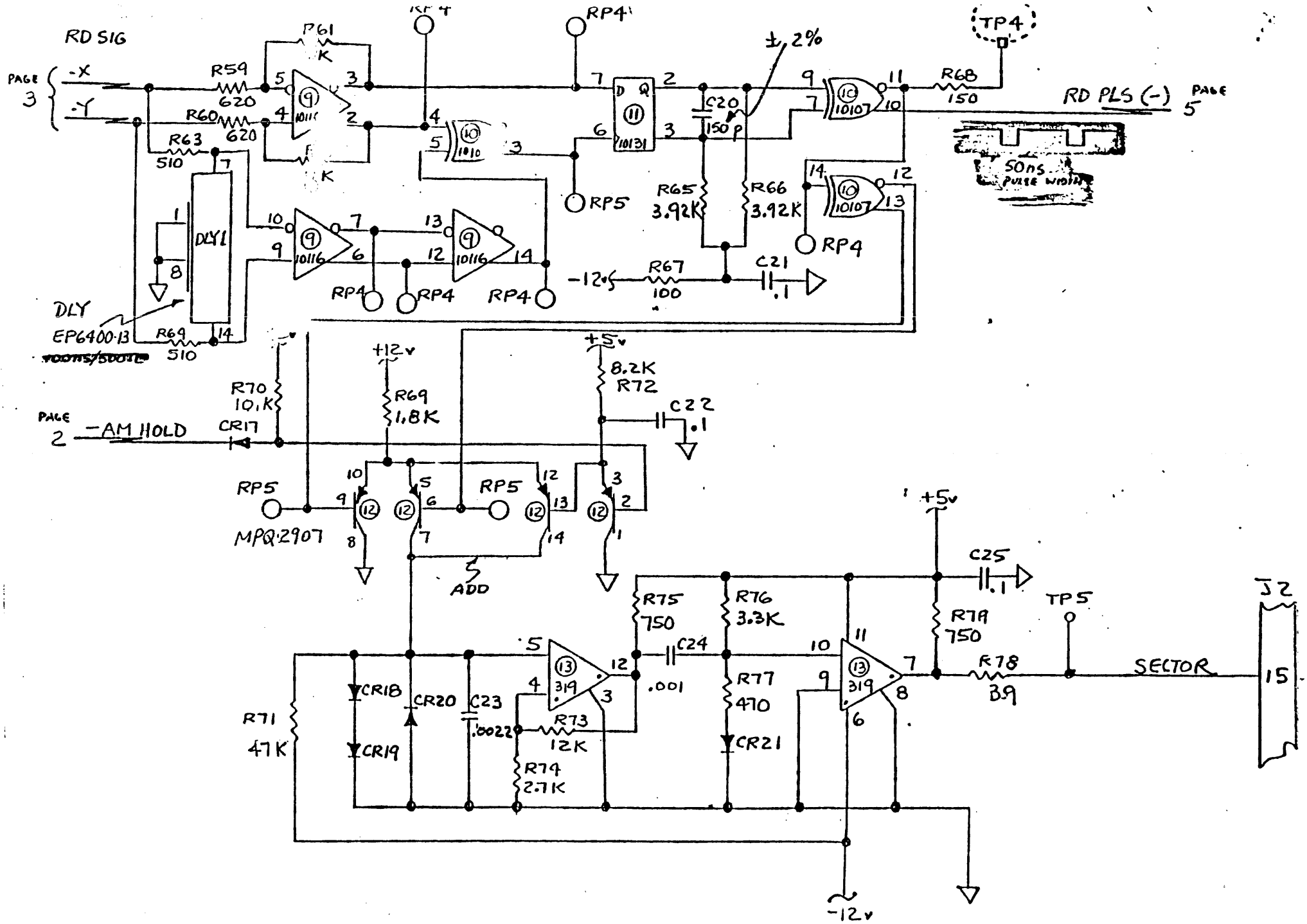
The VCO output is approximately 20Mhz, and is routed to UC22 on page 5. This is a divide by 4 circuit and the resulting 5Mhz signal is the 200nsec VCO "window" into which the incoming read data is locked.

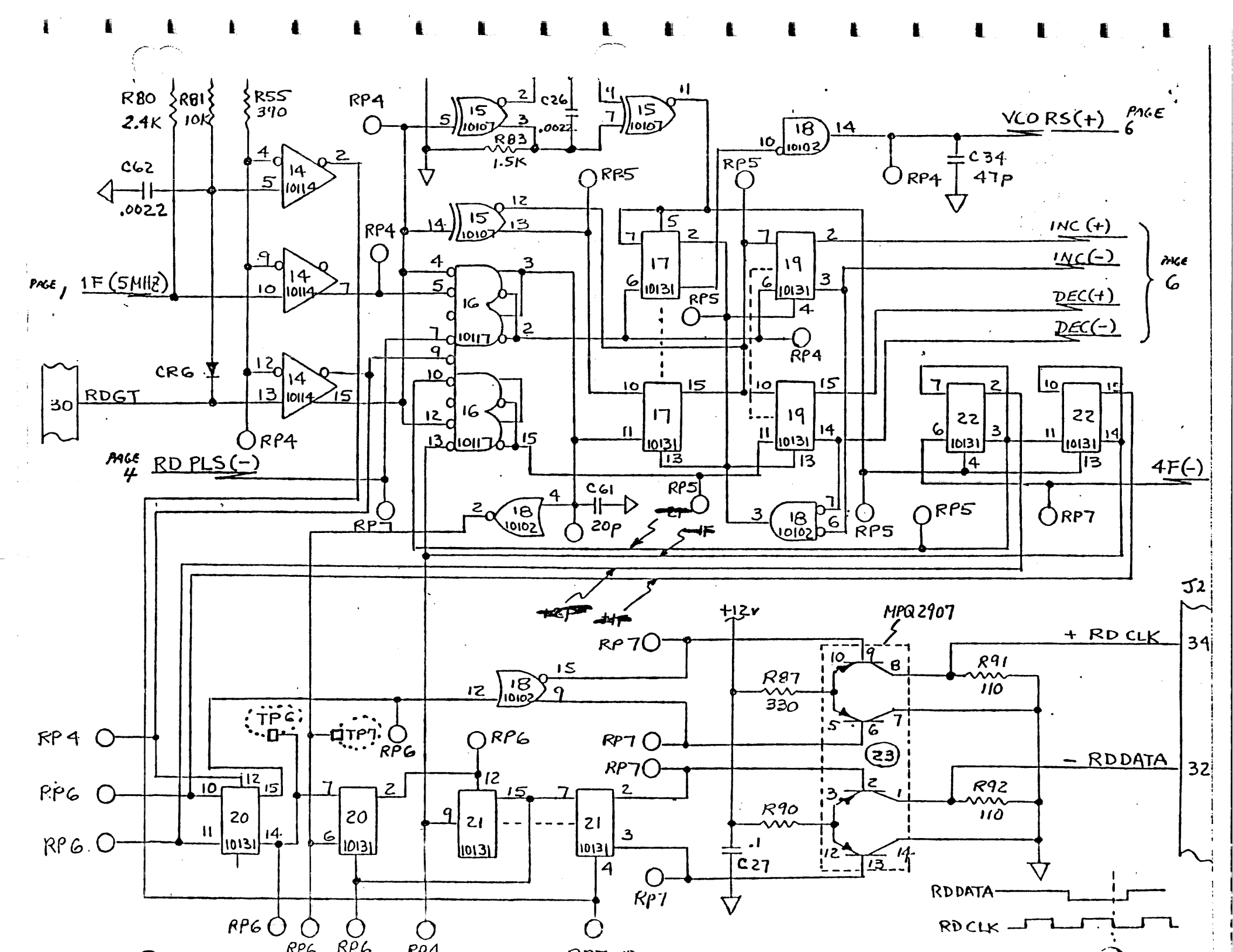

PAL 16RG
(ELY)
(OT)
(LTE)
74S64
DLY 2
EP19824
(50ns/100ns)
R110 200
R111 300
R112 39
R113 3.9K
+5v
RS
WXS
J2
NRZWDTA
2E (10 MHZ)
PCOMP-LOCUR
WTGT
IF (5MHZ)
PAGE #
TP 9
TRK 0
INDEX
+ΦA
-ΦA
+ΦB
-ΦB
R115 100K
R114 150
R116 47K
R117 10K
J8
J6
LS14
+5v
+12v
-12v
C40
C39
C38
GRD

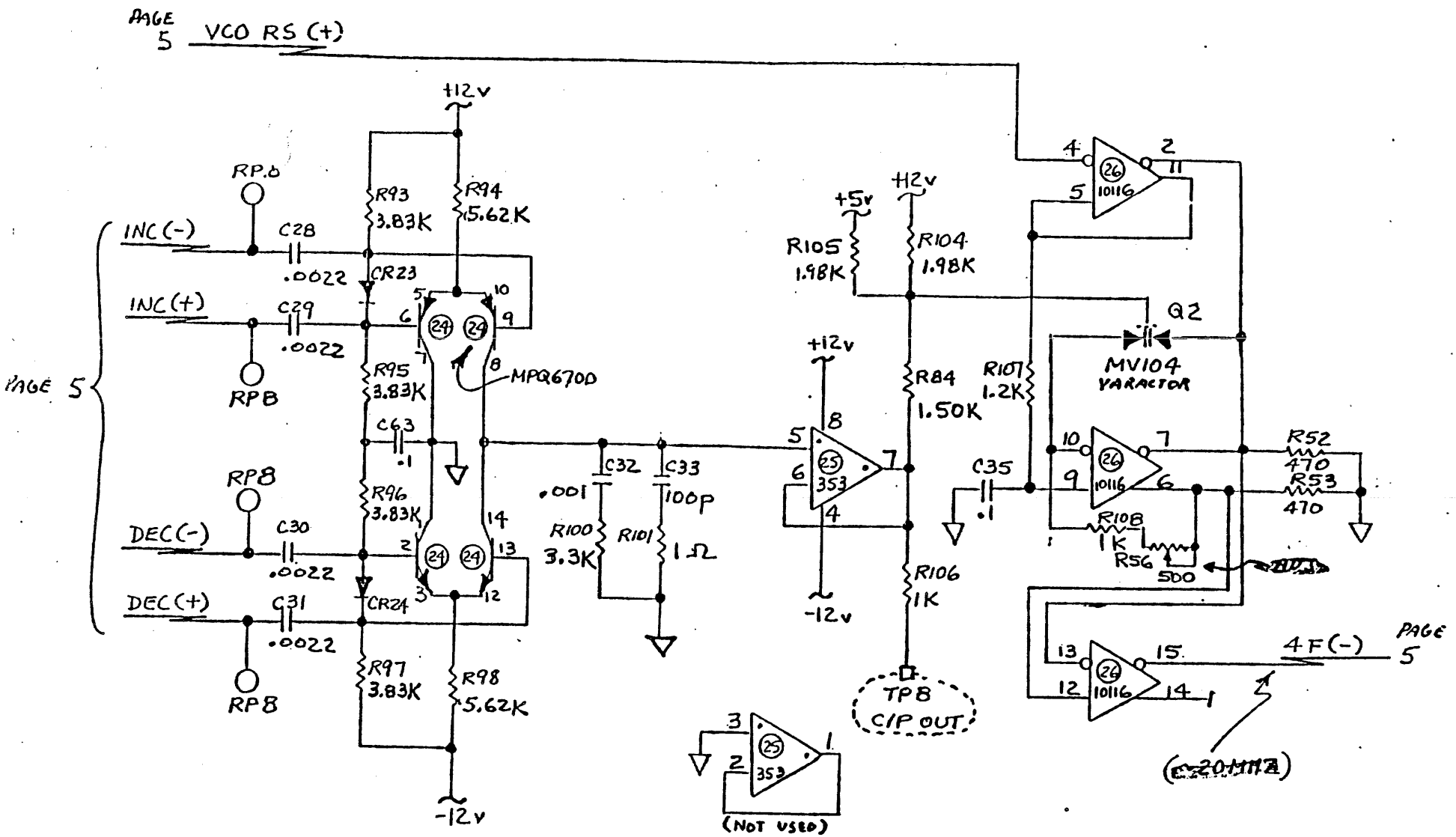
SHEET 1 1 / 0

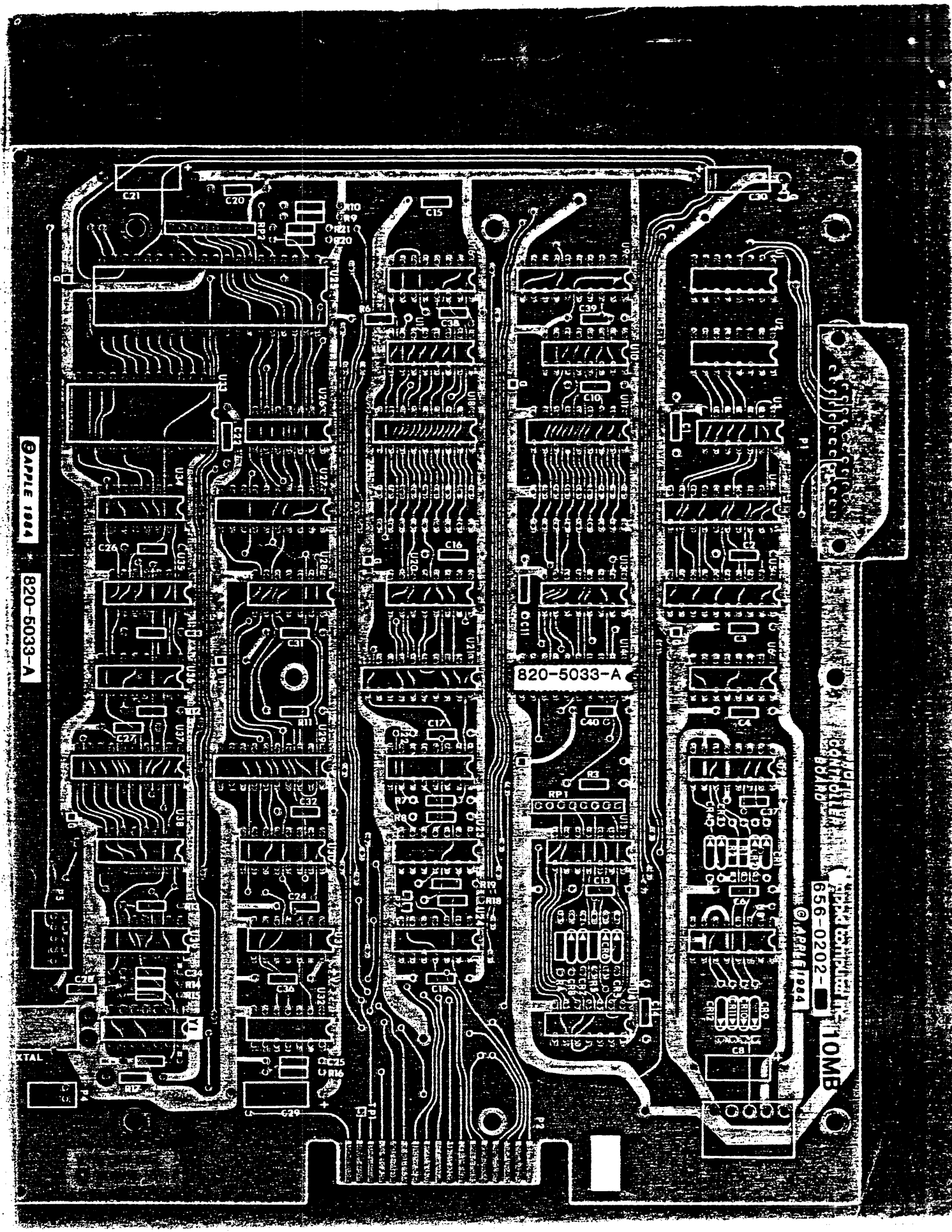

6 POWER
8 WRTSM
R17 10K
C36 .1
R14 45.3
4.7µ
CLK1
C37 .1
R13 10K
R4 100
+12v
MPQ2907
R11
R12 680
R18 240
R19 240
680
R20 1K
+5v
C3 .1
WXS
R21 1K
MPQ6700
R5 7.5K
R6 7.5K
C1 .01
C2 .01
PAGE 3
PAGE 1
WTGT
R27 3.9K
R22 680
R7 1.5K
R9 3.9K
CR4
CR13
R8 3.9K
CR1
CR2
PCOMP-LOCUR
R10 1.78K
+5v
R15 1K
75453
R23 22
R24 22
A
B
C
D
CR4
CR3
+12v
4.7K
RP 1
CR12
CR11
CR10
CR9
CR8
CR7
CR6
CR5
J5
HD-3
HD-2
HD-1
HD-0
J2
28 HS-1
26 HS-0
7445
AM HOLD
PAGE 4


PAGE 2
R1 3.9K
R2 1K
R3 1K
C4 .1
C5 .1
C6 .01
C7 .01
RG1
OUT
IN
+12V
L1 5.6μH
L2 5.6μH
C8 75P
C9 150P
R25 120
R26 120
R28 510
R29 510
R30 510
R31 240K
C10 .1
C11 .1
C12 .1
R32 22
C13 .01
C14 .01
R33 7.5K
R34 7.5K
Q3 VCR2N
CR16
R85 1K
R86 1K
R87 1K
R88 1K
+5V
C16 .1
⑦:CA3127
CA3127E
R36 100
R37 390
R38 1K
R39 1K
C15 .1
R40 1.5K
R41 1.5K
R42 10K
R43 10K
R44 10K
R45 10K
R46 82K
C17 150P
C18 150
R47 10K
R49 10K
R50 20K
C19 .0022
R35 24K
E
F
-12V
JUMPER FOR FIXED GAIN (TEST PURPOSES ONLY)
RDSIG -X
-Y
PAGE 4
TP1
TP2


RD SIG
PAGE 3
-X
-Y
R59 620
R60 620
R61 1K
R63 510
R69 510
DLY
EP6400-13
DLY1
RP4
RP5
±2%
C20 150 P
R65 3.92K
R66 3.92K
R67 100
-12v
C21 .1
TP4
R68 150
RD PLS (-)
PAGE 5
50ns PULSE WIDTH
+12v
+5v
R70 10.1K
R69 1.8K
8.2K R72
C22 .1
PAGE 2
-AM HOLD
CR17
MPQ2907
ADD
R75 750
R76 3.3K
C24 .001
R77 470
R73 12K
R74 2.7K
R71 47K
CR18
CR19
CR20
C23 .0022
CR21
C25 .1
R79 750
R78 39
TP5
SECTOR
J2
15


R80 2.4K
R81 10K
R55 390
C62 .0022
RP4
C26 .0022
R83 1.5K
RP5
VCO RS(+)
PAGE 6
C34 47P
INC (+)
INC (-)
DEC (+)
DEC (-)
PAGE 6
PAGE 1 1F (5MHz)
CR6
30 RDGT
PAGE 4 RD PLS (-)
C61 20P
4F(-)
RP7
1F
+12V
MPQ2907
J2
+ RD CLK
34
R91 110
R87 330
R90
R92 110
.1 C27
- RDDATA
32
TP6
TP7
RP6
RDDATA
RD CLK


PAGE 5 VCO RS (+)
+12V
RP.6
R93 3.83K
R94 5.62K
INC (-)
C28 .0022
CR23
INC (+)
C29 .0022
RP8
R95 3.83K
MPQ6700
C63 .1
RP8
R96 3.83K
DEC (-)
C30 .0022
DEC (+)
C31 .0022
CR24
RP8
R97 3.83K
R98 5.62K
-12V
C32 .001
C33 100P
R100 3.3K
R101 1Ω
+5V
+12V
R105 1.98K
R104 1.98K
R84 1.50K
R106 1K
-12V
TP8 C/P OUT
3 2 1 353
(NOT USED)
4 5 2 11 26 10116
Q2
MV104 VARACTOR
R107 1.2K
C35 .1
10 9 7 6 26 10116
R52 470
R53 470
R108 1K
R56 500
13 12 15 14 26 10116
4F (-)
PAGE 5
(~20MA)
REV DATE: 5/5/81
DPJ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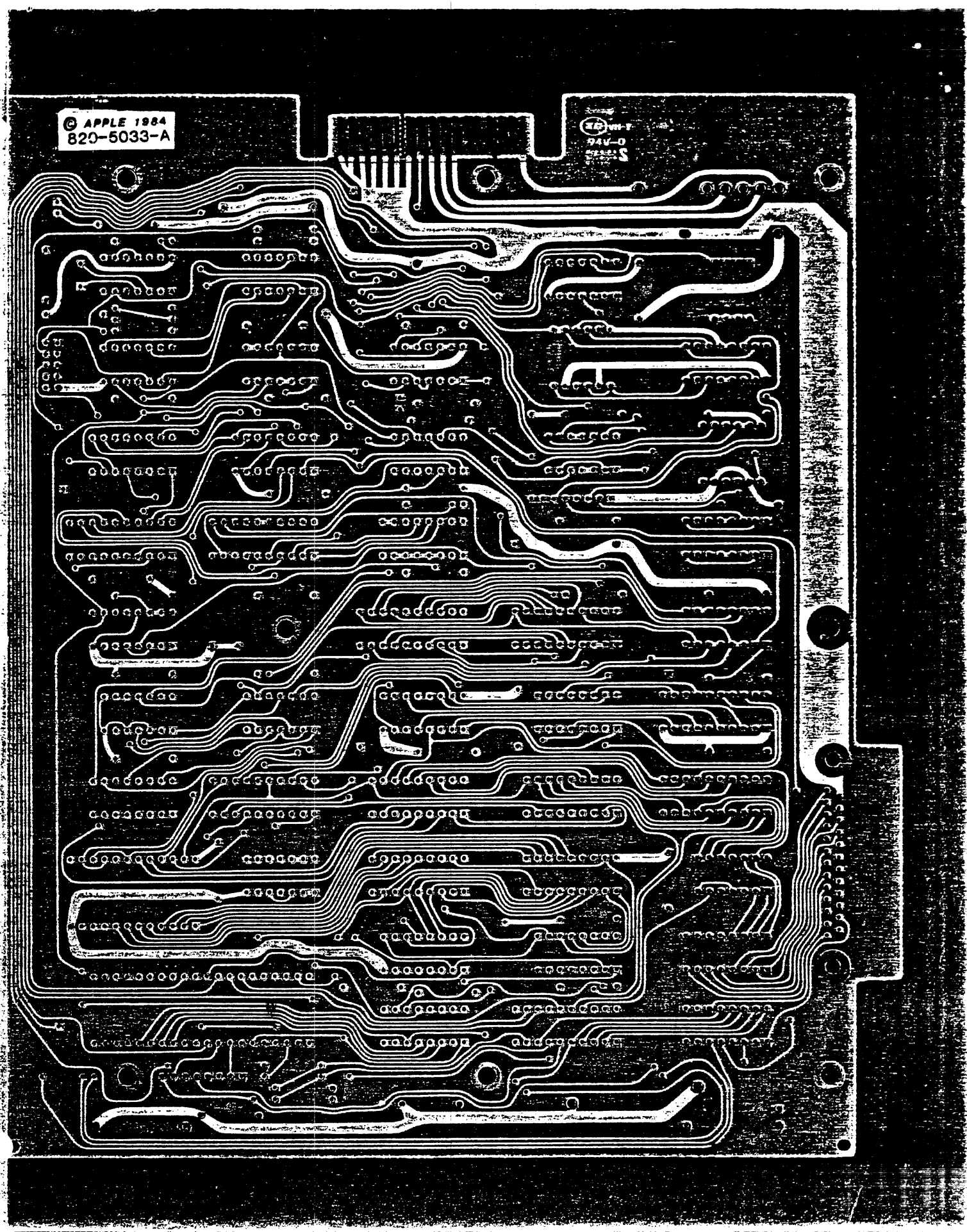
656-0202-
©APPLE 1984
10MB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820-5033-A
94V-0

PROFILE ANALOG BOARD
656-0201-E © APPLE 1984
820-5019-A
656-0207
© APPLE 1984

© APPLE 1984
820-5019-A

REV.	ZONE	ECO #	REVISION	APPD
A		P109	INITIAL RELEASE	
B		P181	Revised to include Monitor CRT and Mechanical Equivalency	

This assembly meets Apple Computer Specification #062-0074, and includes the equivalent circuitry for Apple assy #656-4106, "PCB, Assy, Monitor", Tested, is mechanically equivalent to #656-5102, "Subassy, Power Supply", and is purchased only from U.S. ASTEC as ASTEC part number AA11771.

699-0059-B

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY DATE: Jamie Frederick 8-81
CHECKED BY DATE: 3-30-82
APPROVED BY DATE: 83184
RELEASED BY DATE:

apple computer inc.

TITLE
Purchased Assembly
Power Supply, PROFILE

MATERIAL:

SIZE: A

DRAWING NUMBER: 699-0059-B

NEXT ASSY.

FINISH:

SCALE:

SHEET 1 OF 1

CLASS "A"

REV.	ZONE	ECO #	REVISION	APPD
A		806	INITIAL RELEASE	
B		P120	Deleted pg. 4, AC Line Monitor Elec. Req.; also pgs. 7-9, dwgs & schematic	
C		P171	Dimension change (page 6) 3.75 was 3.65	

1.0 ELECTRICAL CHARACTERISTICS

1.1 INPUT VOLTAGE: 115 VAC or 230 VAC
Selected by jumper on pcb.
47 to 63 Hz

1.2 OPERATING RANGE: 90 to 135 VAC RMS
180 to 270 VAC RMS

1.3 CONVERSION EFFICIENCY: 75% minimum acceptable; with 78% as a target in production.

1.4 DELIVERED POWER: 30 watts steady state.
55 watts starting for a minimum of 14 seconds.

1.5 OUTPUT VOLTAGES AND CURRENTS:

$Vout_1$ +12 VDC ± 6% 1.5 Adc steady state and 3.5 to 4.0 amps for 10 - 14 seconds.

$Vout_2$ +5 VDC ± 2% 2.0 Adc continuous.

$Vout_3$ -12 VDC ± 6% 0.1 Adc continuous.

1.6 RIPPLE AND NOISE CONTENT; OUTPUT: 50MVP-Pon +5VDC;100MV P-P, +12 VDC. 1Hz to 10 MHz.

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DECIMALS .X ± —— .XX ± —— .XXX ± —— ANGLES XX.X ± —— FRACTIONS ± —— DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.	DRAWN BY [illegible] DATE 7-7-81	apple computer inc.	
	CHECKED BY MG DATE 7-81	TITLE POWER SUPPLY, PROFILE	
	APPROVED BY W. Dirks DATE 7/7/81		
	RELEASED BY [signature] DATE 7/8/81	SIZE A	DRAWING NUMBER 062-0074-C
MATERIAL: ——			
NEXT ASSY.	FINISH: ——	SCALE: ——	SHEET 1 OF 6

CLASS "A"

1.7 OPERATING TEMPERATURE: 0 to +70 ^{o}C (Ambient)

1.8 STORAGE TEMPERATURE: -20 to +85^{o}C.

1.9 PROTECTION CIRCUITS: The input must be protected by a fast blow fuse and a thermister inrush current limiter.

The +5 volts d.c. TTL voltage must be protected from over voltage output by means of an active crowbar.

All three d.c. outputs must be short circuit capable for an indefinite period.

1.9.1 HOLD UP TIME: 20 msec nominal at 30 watts load.

1.9.2 TEMPERATURE COEFFICIENT: 0.02%.

1.9.3 AC ISOLATION: to safety ground and A.C. input to output 4.5KVDC

1.9.4 OUTPUT TO SAFETY GROUND: 0.5KVDC

1.9.5 INSULATION AC TO GROUND: 50 MEG ohm nominal.

1.9.6 LEAKAGE CURRENT: 240 VAC input
IRMS $\leq$ 3.5 ma RMS

1.9.7 LINE CONDUCTED EMI: FCC 20780 limits. See attached specifications

1.9.8 SAFETY APPROVALS: UL and CSA required.
VDE required after 9/81.

2.0 MECHANICAL REQUIREMENTS:
The supply shall conform to attached envelope.

2.1 THERMAL: The power supply shall be capable of operating under all conditions of line and load at 0-70^{o}C continuously.

2.2 STORAGE TEMPERATURE: -20 to +85^{o}C.

2.3 HUMIDITY: Operating: 95% RH @ 35^{o}C.
Storage: 95% RH @ 50^{o}C.

2.4 VIBRATION: 10 to 500 Hz double sweep at 1 active per minute with pk-pk excursion of 1.5mm or 10g acceleration.

2.5 RANDOM DROP: 45 min. at a rate of 5 RPM.

2.6 BURN IN: A minimum 24 hour burn in at low line, full DC load at 70^{o}C is required. Vendor will burn in all units.

2.7 SERIALIZATION: All supplies shall have a serial number affixed and recorded so that test and failure records can be tracked throughout the life of the product.

2.8 SAFETY REQUIREMENTS: UL 478
UL 1201
CSA 22.2 No. 154
VDE after 9/81

2.9 INDUCTORS

No solenoidal filter inductors should be used in this product.

2.95 INPUT AND OUTPUT CONNECTOR: Molex Connector Pin Designation.

A.C. Input	D.C. Connector
1. AC Neutral	1. Reset Monitor Output
2. Key	2. Key
3. AC Line	3. -12V
	4. +12V
	5. +12V
	6. Common
	7. "
	8. "
	9. "
	10. Common
	11. +5V
	12. +5V
	13. +5V

Mating Molex Connectors:

DC P/N 09-50-3131

AC P/N 09-50-3030

The output connector will be a single, in-line connector combining the above two part numbers.

SPECIFICATION: ELECTROMAGNETIC COMPATIBILITY

1. Emissions: Applicable assemblies, subassemblies and peripheral devices shall be 6 dB below limits of (1) Federal Communications Commission (FCC) Part 15 Sections 15.830 (radiation limit) and 15.832 (conduction limit) for units operated from 60 Hz line voltage and (2) VDE 0871/6.78 section 3.2.1 (conducted) and sections 3.2.2 and 3.2.3 (radiated) for units operated from 50 Hz line voltage. Those units rated 50/60 Hz shall meet both requirements.

   The upper frequency limit for both FCC and VDE conducted emissions limits is 30 MHz. However, due to radiated emissions from the AC power cord the Apple conducted limit is extended to 60 MHz.

   For convenience, limit amplitudes, less 6 dB, are reproduced herein. (Tabulated limits are Apple Computer EMI limits; FCC and VDE limits are 6 dB higher). However, the in-effect version of FCC part 15 or VDE 0871 are the binding documents.

   RADIATED

	Frequency Range (MHz)	Field (uV/m)	Strengths (dB uV)	Distance (meters)
1. FCC Part 15	30-88	50	34	3
	88-216	75	38	3
	216-1,000	100	40	3
2. VDE 0871	0.01-30	20	26	30
	30-470	20	26	10
	470-1,000	80	38	10

   CONDUCTED

	Frequency Range (MHz)	Voltage (uV)	(dB uV)	LISN Impedance
1. FCC Part 15	0.45-60	125	42	50
2. VDE 0871/6.78	0.01-0.15	*		150
	0.15-0.50	200	46	
	0.50-60	100	40	

   *straight line from 10 kHz (3.5mV, 71 dB V) to 150 kHz (300uV, 50 dBuV)

   Test and measurement equipment and procedures shall be as specified in applicable specifications. Final acceptance tests are performed with assembly or peripheral installed in system intended to be marketed with; such system to consist of the basic Apple Computer (II, III, etc.) and full memory installed and as many peripheral devices (disk drives, printer, monitors) and optional components (language card, serial card, parallel card, etc.) as possible to simulate worst-case operating conditions as closely as possible. Qualification tests with "remote exercisers", generators or other manufacturer Personal CPUs are unacceptable.

II. SUSCEPTIBILITY (to be determined).

   Under consideration: The device shall not have uncorrectable data errors when subjected to the following field strengths or voltages - Irradiated: 0.01-1,000 MHz, 5V/m (100% modulated with 1 kHz square wave).

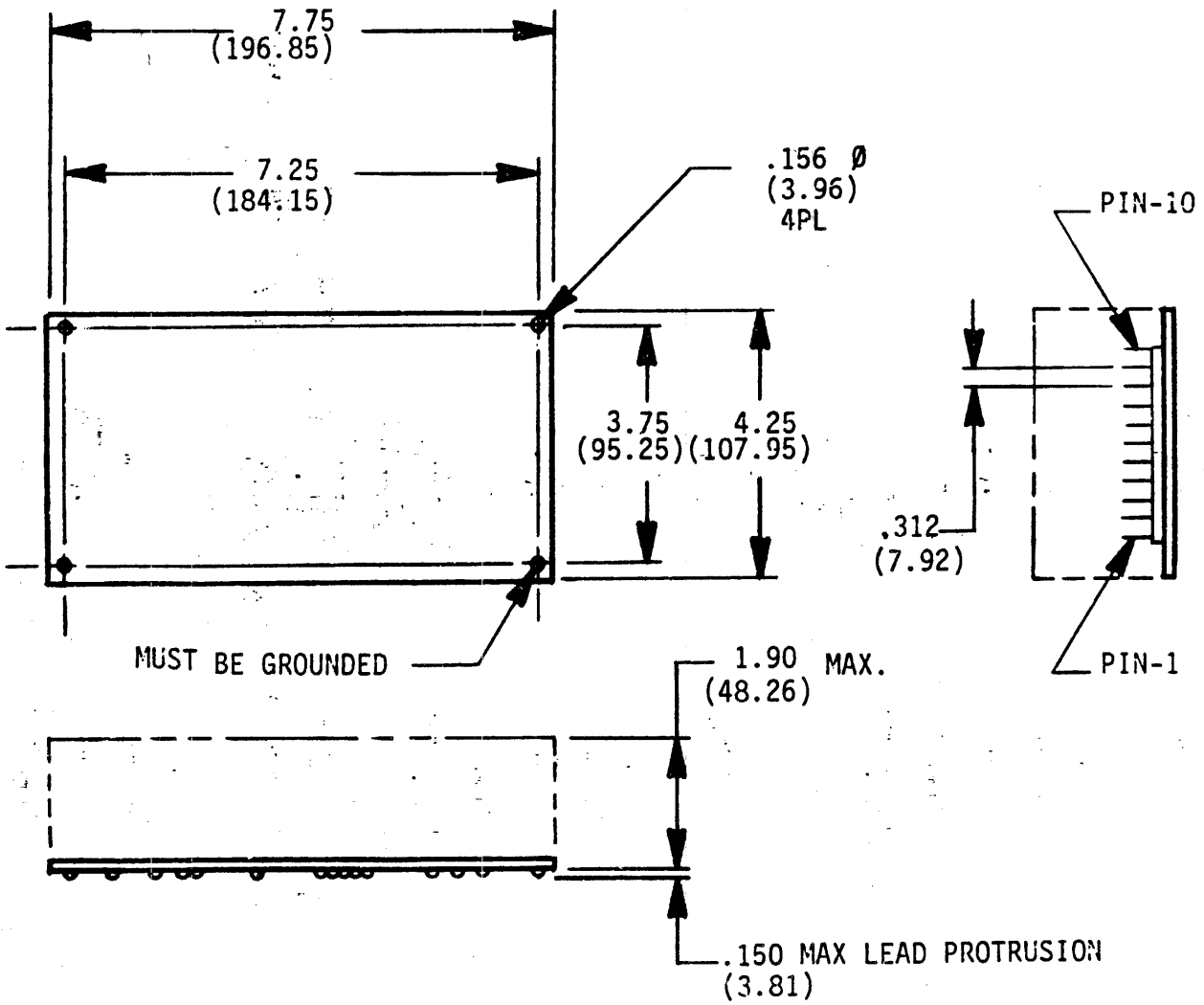
II. SUSCEPTIBILITY (to be determined) - continued.

Transient Line Noise:** 1. Class A products: 400V pulse with 100 nonosecond width and 10 nsec risetime.

2. Class B products: 200V pulse (same characteristics)

Conducted RF: 0.01-100 MHz: 3V rms.

**no soft errors allowed.



apple computer inc.

SIZE	DRAWING NUMBER
A	062-0074-C
SCALE: ——	SHEET 6 OF 6

REVISIONS				
MLC		DESCRIPTION	INC BY	APPROVAL & DATE

APPLICABLE DOCUMENTS

Motor Control PCB Assembly 20217-001

Engineering Specifications:

The HDA components shall meet all requirements and specifications set forth in the following documents unless separately specified herein.

Motor Control PCB (Fab drawing)	20218-001
HDA Assembly drawing	58157-001
HDS Electrical interconnect drawing	
Magnetic Disc	30126-001
Read/Write Heads	30134-001
Head Connector	10420-016
Spindle Motor Connector	10417-006
Stepper Motor Connector	10417-005
Index Connector	10417-005

DWG. NO.

MODEL NO. FIRST USE	ST-412.9	NEXT ASSY FIRST USE	FINAL ASSY

DRAWN		
CHECK		
APPD(E)		
APPD(M)	[illegible]	1.19.81

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .XX .XXX
ANGLES ±

SEAGATE TECHNOLOGY

ST412.9 HEAD DISC ASSEMBLY

SCALE	SIZE	DWG NO.	REV. EC
	A	30173-001	0292

DO NOT SCALE

APPLICABLE DOCUMENTS (continued)

TK Ø Connector	10417-005
Spin Motor PCB Connector	10419-002
10416-XXX (Ref) Mates with	10417-XXX
10415-XXX (Ref) " "	10420-XXX
10418-XXX (Ref) " "	10419-XXX
Shock & Vibration Spec.	30138-001
Acoustical Specification	30131-001
Shock & Vibration Spec.	30138-001

CONTENTS

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III. MEDIA

IV. ENVIRONMENTAL

V. RELIABILITY

VI. POWER

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X. SPINDLE MOTOR - ELECTRICAL REQUIREMENTS

XI. BAND ASM - MECHANICAL REQUIREMENTS

XII. PHYSICAL REQUIREMENTS

I. SCOPE

The Head Disc Assembly (HDA) is a sub-assembly of the ST412.9 Final Disc Drive Assembly. It will undergo all the drive testing before being shipped to the customer. The Head Disc Assembly will be a complete ST412.9 disc drive less the following hardware:

1) Main control PCB

2) Front panel

II. CAPACITY

Unformatted

Mbytes/Drive	12.76
Bytes/Track	10416

Formatted 32 Sectors/Track (Soft)

Mbytes/Drive	10.0
Bytes/Track	8192

	Max recording frequency (MHZ)	2.5
	Transfer Rate	
	Mbits/Second	5.0
	Density	
	Flux Changes/Inch	9074

III. MEDIA

Tracks	
Per Inch	345
Per Surface	306
Per Drive	1224
Defects (Hard Errors)	
Per Drive	12
Per Cylinder Zero	0

IV. ENVIRONMENTAL

	Operating	Shipping	Storage
Ambient Temperature*	39° - 135°F 10° - 50	25° - 144°F -4° - 62°C	-8° - 176° -22°C- 80°
Max Temperature Gradient/Hour	18°F	18°F	18°
Relative Humidity	20 - 80%	TBD	TBD
Maximum Wet Bulb	78°	No Condensation	
Stray Magnetic Field	(1" from casting)	20 Gauss Max	
Altitude		10,000 ft. Max	

* Ambient Temperature is defined as the HDA casting temperature.

V. RELIABILITY

Error Rate (Excluding defects) - When used with Seagate Technology PCB P/N TBD.

Soft read errors (16 retries min.)	1 per 10^{10} bits transferred
Hard read errors	1 per 10^{12} bits transferred
Seek errors	1 per 10^{6} seeks
MTBF (Meantime before failure)	
Typical usage	11,000 hours
PM (Preventive Maintenance)	None
MTTR (Meantime to Repair)	30 minutes
Component Life	5 years
Media Life	10,000 starts/stops

VI. POWER

DC Voltages (To motor speed control)

+12 VDC ± 10%, .8 AMP running current; 2.7 AMPs typical motor start current. (see ST412 manual for start profile).

BTU/Hr. (1 watt = 3.413 BTU/Hr.)

Watts	25	± 40%
BTU/Hr.	85.3	± 40%

VII. INTERFACE

TBD.

VIII. DRIVE

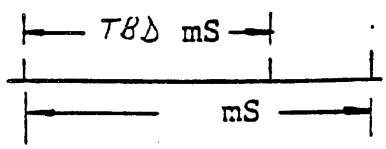
A. Mechanical

Seek Settle Time*

Uncontrolled TBD

Controlled TBD using this step sequence

Track to Track (Seek = 3 ms)



* Using Seagate recommended PCB

Drive Motor Start Time — 15 sec.

Spindle Speed** — 3600 rpm ± 1%

HDA Cleanliness

The air inside the HDA shall be class 100 (0.5) micron particles)

Mounting

See Figures 1 & 2

Vibration and Shock

Shall meet the requirements of Seagate Specification 30138-001

B. Electricial

For purposes of normalized test data, and unless otherwise stated, all test measurements shall be taken at the ambient conditions of 68 + 5°F (20 + 3°C) and 40 to 60% relative humidity after the HDA has been stabilized at the test environment for at least 1 hour.

Not withstanding this, the HDA shall be capable of meeting all the requirements of this specification over the full operating environment of Paragraph IV, Page 4.

Warm Up Time

The HDA shall meet all operating specifications within 15 seconds after spindle motor has reached 3600 RPM at all operational environmental conditions.

1. Spindle motor speed regulation — 3600 ± 1% RPM
2. Spindle motor current

Start	2.75amps max.
Running	1.0 amps max.

3. Stepper motor/phase — TBD

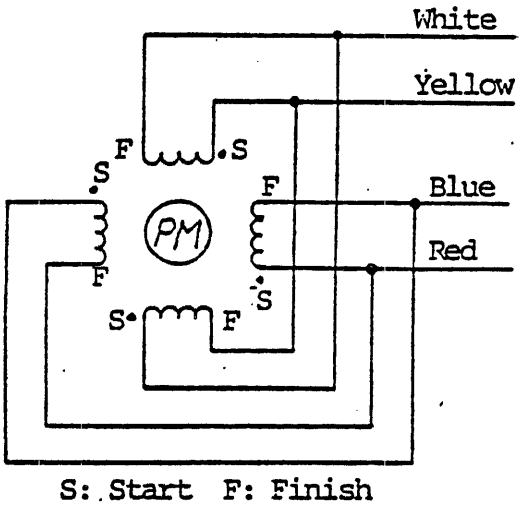
**Adjustments are customer responsibility
***For shipment, the heads shall be moved center track while the spindle is rotating.

4. Performance (Head Disc Asm)

Average 2F amplitude	1.0 mv p-p min.
Inside window margin (without write precomp)	30 ns total
Minimum resolution on any track (without precomp.)	60%

Wide Gap Measurement

1. DC erase tracks 303, 304, 305
2. Write 2F on track 304
3. Write 1F on tracks 303 & 305
4. Measure 1F amplitude relative to 2F amplitude on track 151 using H.P. spectrum analyzer Model No. 3585A or equivalent.
5. Failure is defined as a measurement $\geq$ - 26dB.



S: Start F: Finish

ELECTRICAL REQUIREMENTS

STEPPER MOTOR

Switching Sequence for CCW Rotation
Facing Mounting End

Step	Pin 4 Blue	Pin 5 Red	Pin 2 White	Pin 1 Yellow	Pin 3 Not Us
1	-	+	+	-	
2	+	-	+	-	
3	+	-	-	+	
4	-	+	-	+	
5	-	+	+	-	

SCHEMATIC

SPECIFICATIONS
Step per revolution: 400 (0.9° per step)
Step to step accuracy (Notes 1,2,): ± 6%
Positional Accuracy (1,3): ± 6%
Rotor Inertia: 20 Gcm^2 (.28 MOISS)
DC Phase Resistance: 38 ± 3.8 at 25° C
Phase Inductance: 27 mH ± 20% at 1 KHZ
Phase Voltage: 9.2
Phase Current (Steady State): 240ma
Holding Torque: 720 gcm (10 oz. - IN) Nom.
Pull-out Torque: 360 gcm (5 oz. - IN) NOM.

NOTES:

1. Measurements made at rated current on each phase.
2. Between any two adjacent step positions.
3. Maximum error in 360°.
4. Motor to be driven bipolar.
   The above specifications is of a motor in bipolar mode.
5. Leads: 4, No. 26 AWG PVC insulation UL & CSA approved.

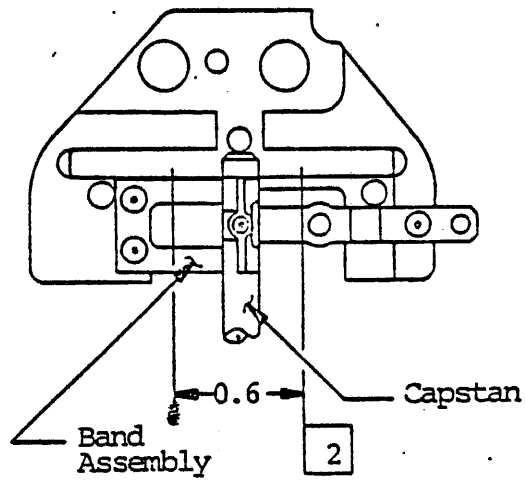
TBD.

IX. PHYSICAL REQUIREMENTS

The HDA can be mounted on any side except upside down or front and back. (See Figures 1 & 2)

The HDA is shock mounted for vibration isolation. In the final mounting configuration, care shall be taken to insure that the operation of the three shock mounts is not restricted.

BAND ASSEMBLY

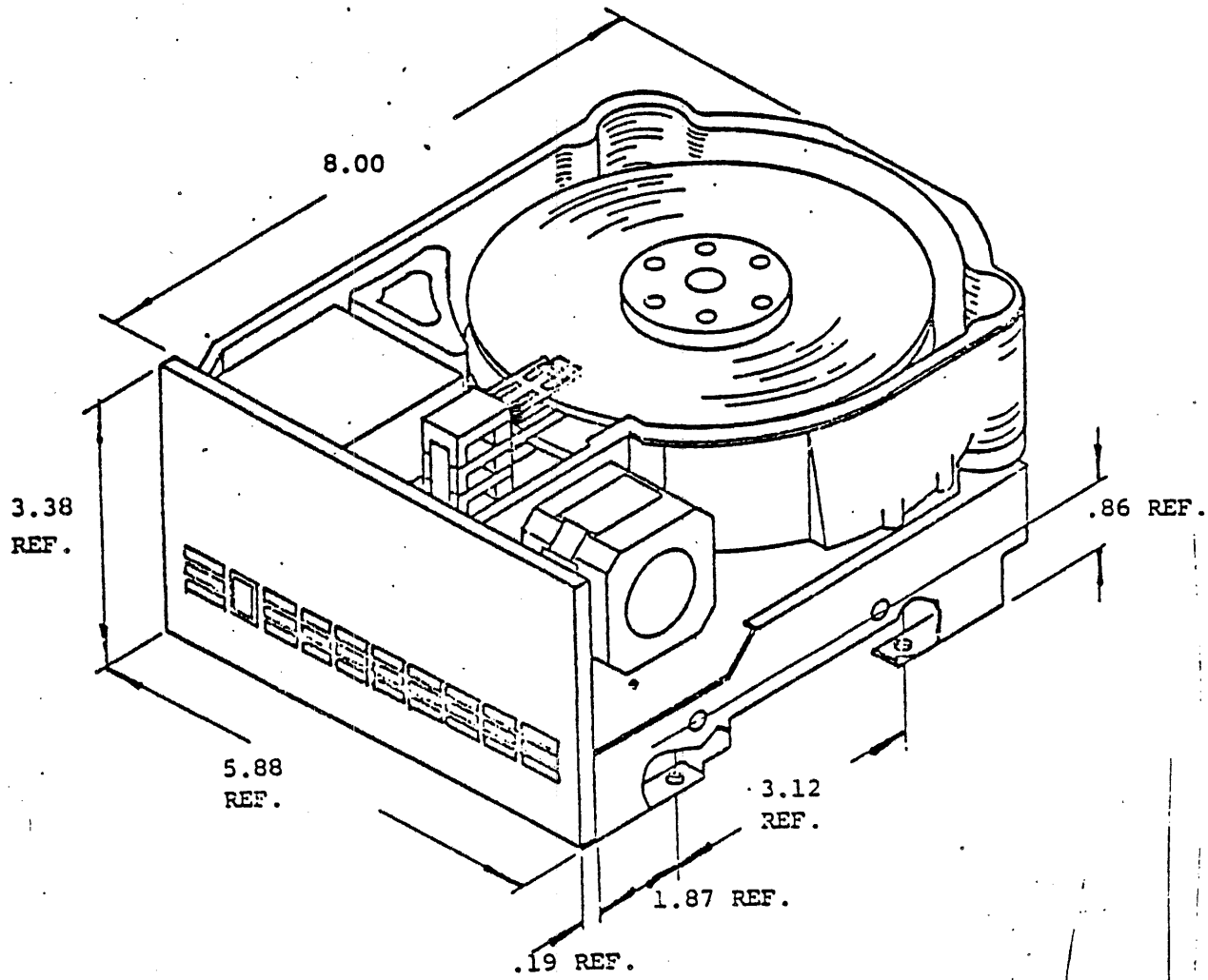


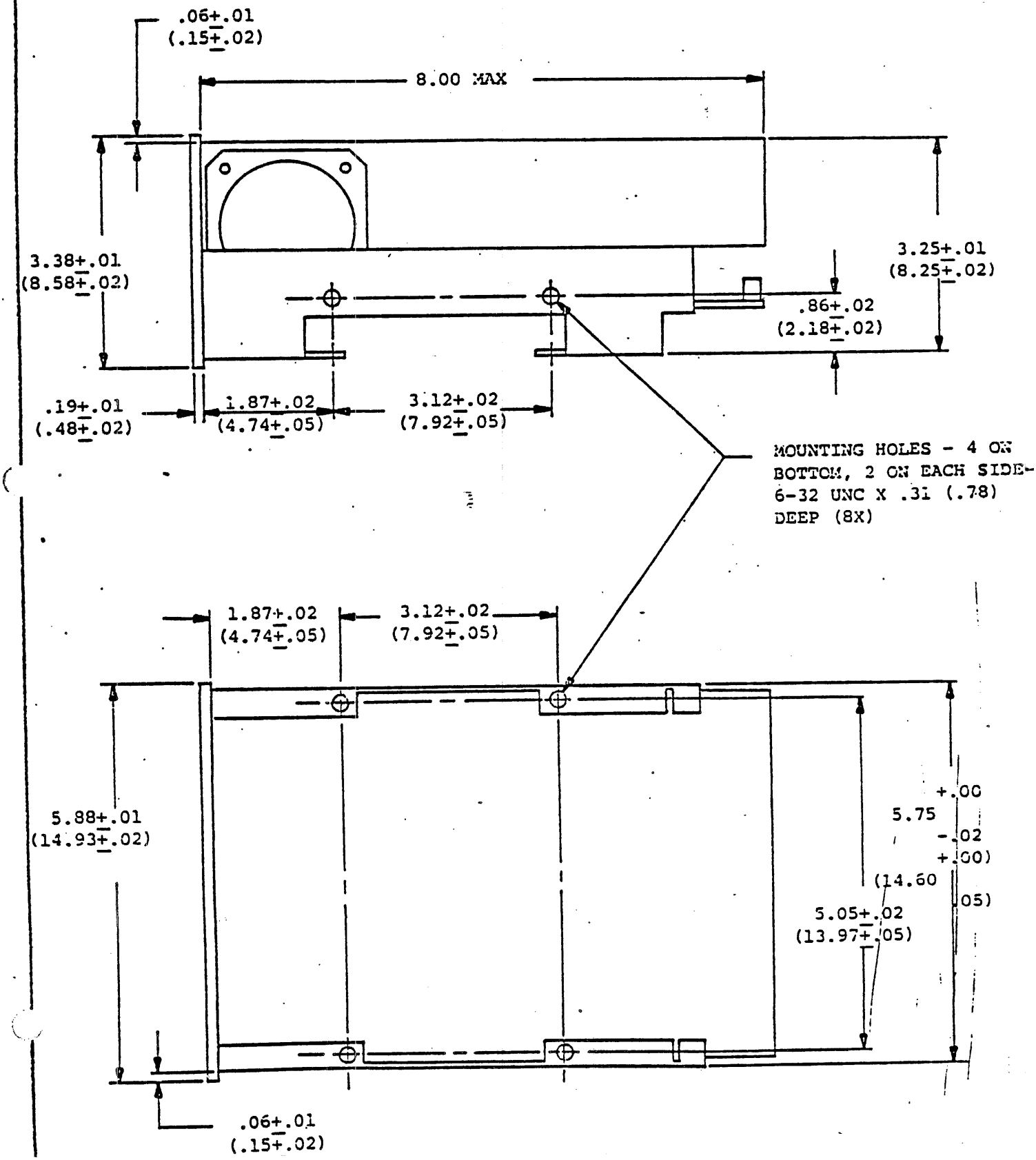
BAND SPECIFICATIONS

1. Band shall be capable of withstanding 2.5 lbs. Max. tension.

2. There shall be no creases on the active portion of the band.

3. Band shall be free of contaminants that would decrease it's life, such as finger prints and edge nicks.


8.00
3.38
REF.
.86 REF.
5.88
REF.
3.12
REF.
1.87 REF.
.19 REF.


.06±.01
(.15±.02)
8.00 MAX
3.38±.01
(8.58±.02)
3.25±.01
(8.25±.02)
.86±.02
(2.18±.02)
.19±.01
(.48±.02)
1.87±.02
(4.74±.05)
3.12±.02
(7.92±.05)
MOUNTING HOLES - 4 ON BOTTOM, 2 ON EACH SIDE-
6-32 UNC X .31 (.78) DEEP (8X)
1.87±.02
(4.74±.05)
3.12±.02
(7.92±.05)
5.88±.01
(14.93±.02)
5.75
+.00
-.02
+.00)
(14.60
05)
5.05±.02
(13.97±.05)
.06±.01
(.15±.02)

5 MEG PROFILE

HDA FORMATTER

(Rev 02/25/83)

Profile Level 2 Technical Procedures

Contents:

Formatting the Profile HDA.....1.3

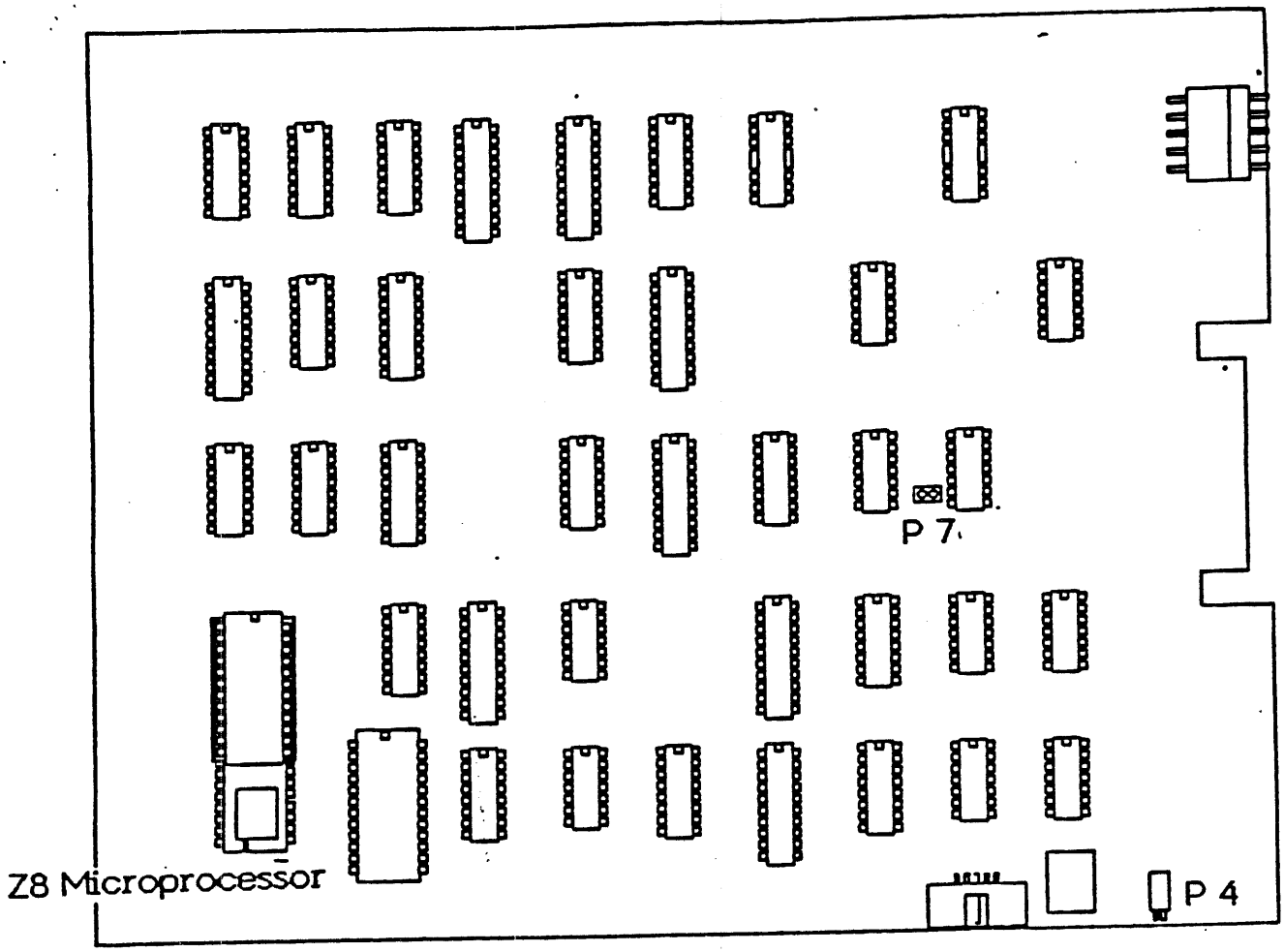


Figure 1 - Profile Controller Board

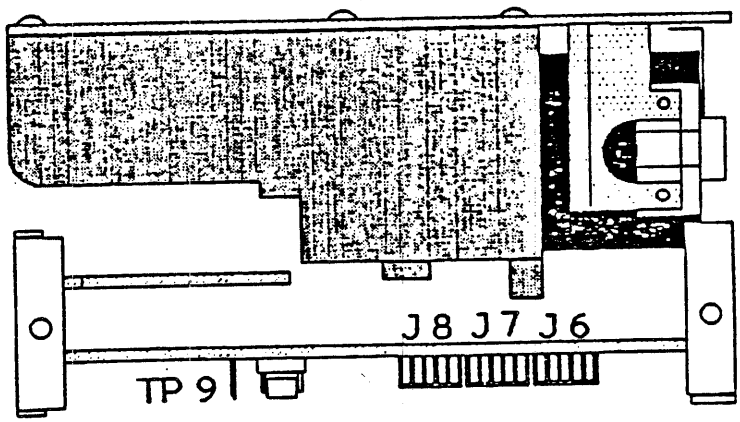


Figure 2 - HDA End View

FORMATTING THE PROFILE HDA

Equipment Necessary:

Format Firmware - Rev 18
Jumper Wire
Profile Format Diskette - Rev 12
Profile Final System Test - Rev 23
Frequency Counter
Small Screwdriver
IC Extractor
Apple /// w/Profile interface and cable
Known good Profile System minus the HDA.

Procedure:

1. Place the HDA to be formatted into a known good Profile system. The controller should contain the piggy-back development type Z8 (shown in Figure 1).

2. Remove the System ROM from the piggy back on the Z8 then install the Format Firmware. Locate the connectors J6, J7 and J8 (shown in Figure 2) that connect the HDA to the analog board. They are a constant source of problems. Move the wires around and make sure that they are securely fastened to the connectors. Connect an external LED to P4 (shown in Figure 1).

3. Power up the Profile and allow 1 minute for the drive speed to stabilize.

4. To check the speed of the HDA, set up the frequency counter to display milliseconds, and connect the input of the frequency counter to TP9 on the analog card. The frequency counter should read 16.67 milliseconds +/- .5%. If it does not, adjust R3, on the side of the HDA (shown in Figure 3) as close to 16.67 milliseconds as possible.

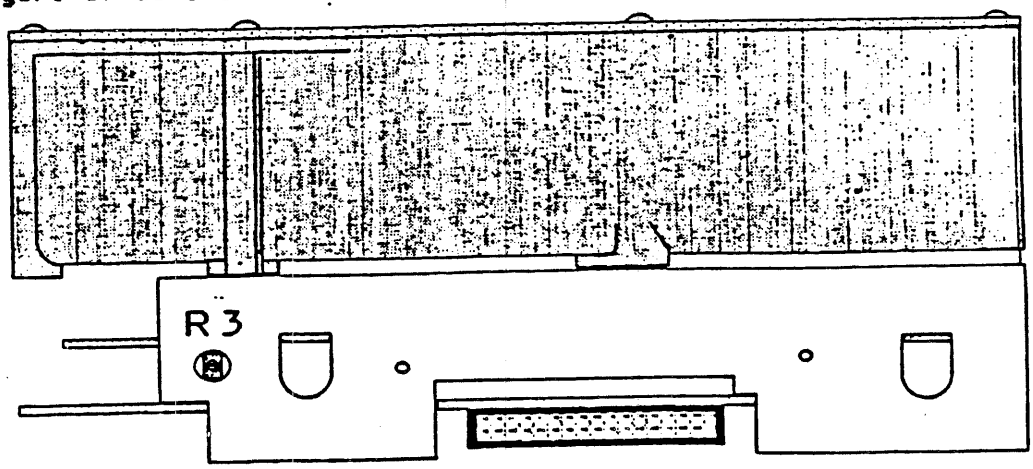


Figure 3 - HDA Side View

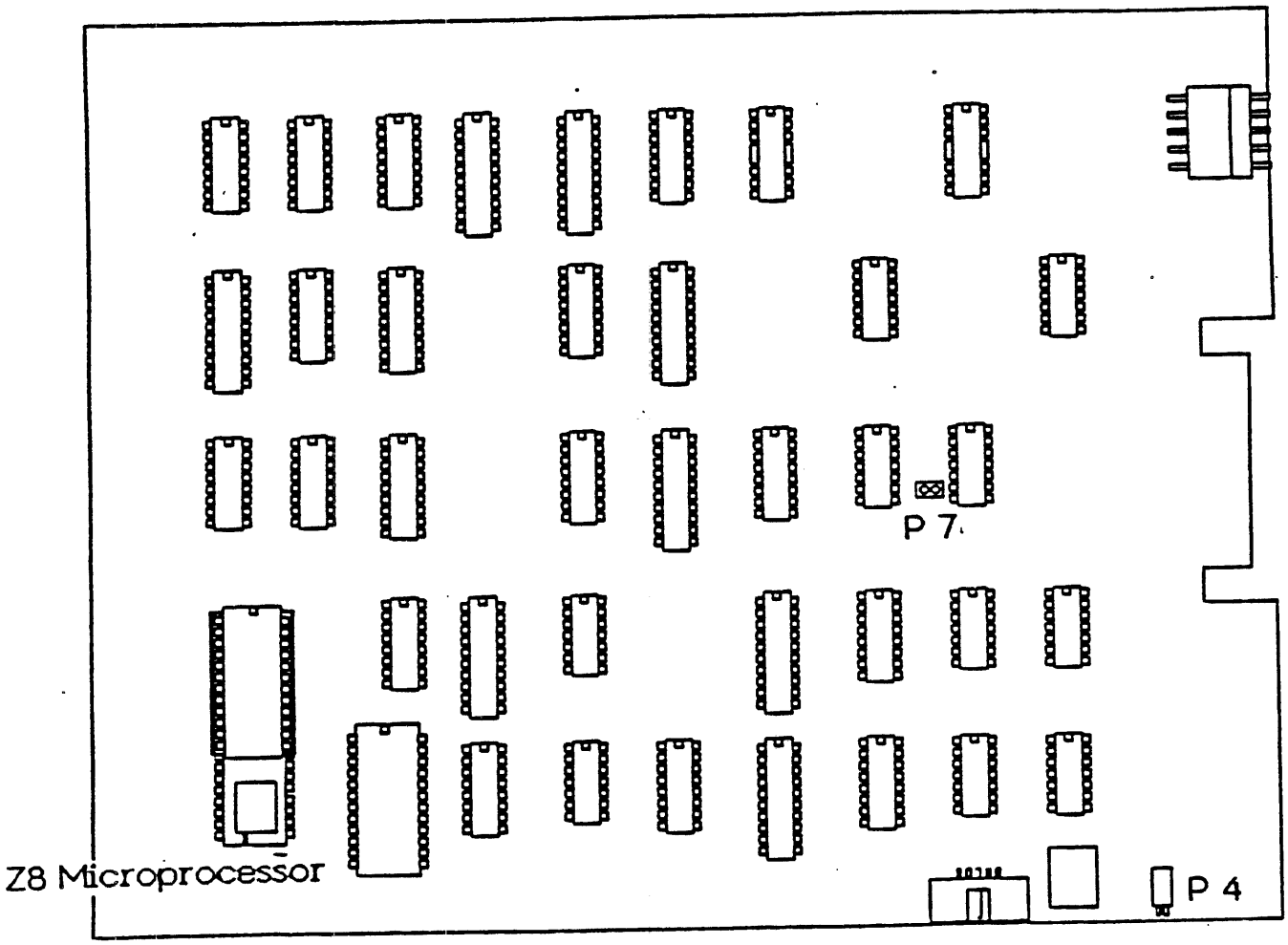


Figure 1 - Profile Controller Board

5. Install the Profile interface card into slot 1, and a Silentype Printer into Port A of the Apple ///. Connect the cable between the interface and the Profile.

6. Boot the Format/Certify Test diskette. When the program is loaded, the following message should appear:

   PRESS "RETURN" WHEN PROFILE IS READY

7. After the <RETURN> key is pressed, the following message will appear:

   INSTALL JUMPER, PRESS ANY KEY TO CONTINUE

8. Install a jumper between the two pins at P7 on the controller card and then press the <RETURN> key. Although the prompt says that you can press any key to continue, only the <RETURN> key will work.

9. When the <RETURN> key is pressed, the LED should start to flash and the stepper motor will step outward. The HDA surface is now being formatted.

10. After approximately 3 minutes, the HDA will be formatted and the following message will appear:

    REMOVE JUMPER, PRESS ANY KEY TO CONTINUE

    Remove the jumper wire from P7 on the controller card. Although the message again states that you may press any key to continue, only the <RETURN> key will work.

11. When the <RETURN> key is pressed the Profile will scan, certify and initialize the spares table on the HDA surface. The results of each process are reported on the printer, ending with the following pass or a fail message for the completion of the test:

    TEST COMPLETED, SYSTEM PASSES <FAILS>

    If the test fails, the HDA is defective and should be returned.

12. Power off the Profile and replace the Format Firmware with the 3.98 System Firmware (P/N 341-0008B) or with the masked Z8 microprocessor (P/N 341-0080B)

13. Power on the Profile, and observe that it goes though the power up sequence. When the LED is steadily on, boot the Profile Final System Test.

14. After the Final Test has booted, observe the printout on the Silentype. The following message is printed:

    CONTROLLER VERSION NO. D3.98

    Directly below, the printer will print:

    SPARE SECTORS BAD BLOCKS
    XX XX

    The number under "SPARE SECTORS" (this should be SPARED SECTORS) is the number of sectors that have already been spared by the Profile. A spared sector is a logical block that has been assigned a new physical location because the old physcial location has reached an unaccectable error rate threshold during transfer operations. There are 32 spare sectors on the Profile that can be used for this purpose.

    The number under "BAD BLOCKS" is the number of blocks that cannot be accessed at all. Any number here indicates a potentally bad Profile. If there are any bad blocks listed here, run the test and match it to the FST Results Chart at the end of this procedure.

15. After a 5 second pause, the final test will begin transferring blocks of data between the Apple /// and the Profile. Figure 1 illustrates the monitor display. The bottom line of the header is the status line, which returns the inforamtion about the current block being transferred. When an error occurs, the status will be printed on the bottom line of the monitor and on the Silentype.

16. After the test has completed 500,000 block transfers (about 24 hours), the test is completed. Use the FST Results Chart on the next page to determine the kinds of errors that have occurred and if the unit has passed or failed.

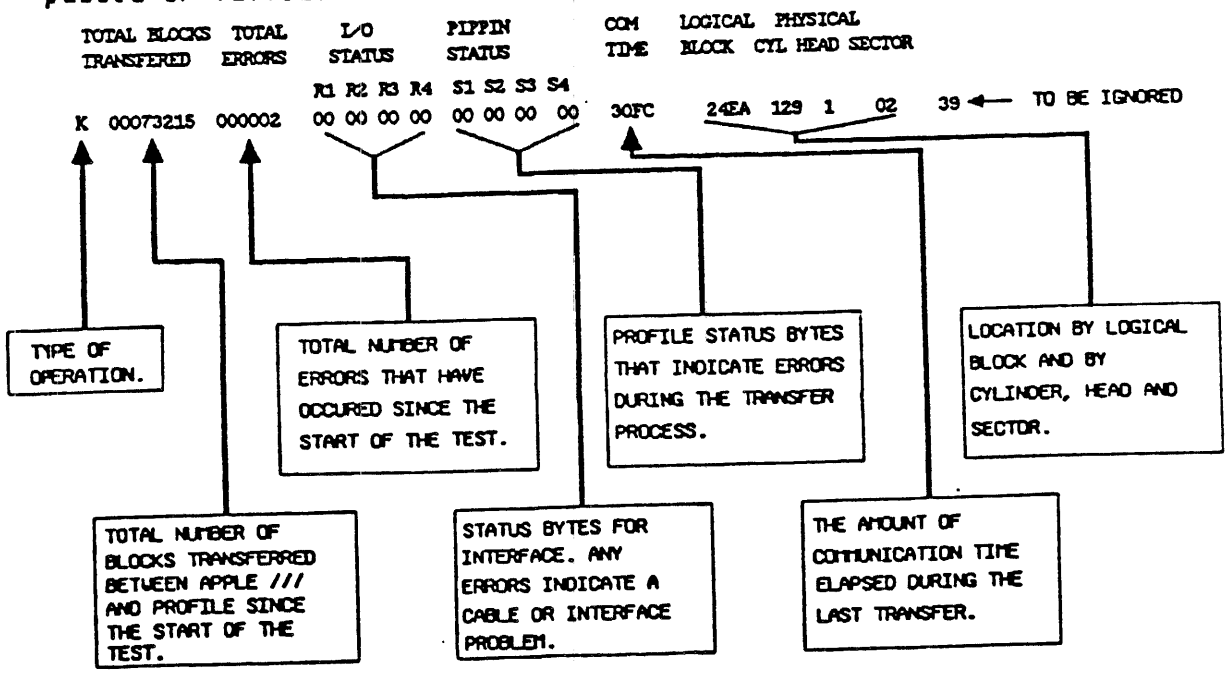


Figure 4

Profile Status Bytes Description

STATUS BYTE 1

7 = 1 if Profile did not receive 55 to its last response
6 = 1 if write or write/verify was aborted because more than 532 bytes of data were sent or Profile could not read the spares table.
5 = 1 if host data is no longer in RAM because Profile updataed its spares table.
4 = 1 if SEEK ERROR - unable in 3 trys to read 3 consecutive headers on a track
3 = 1 if CRC error (only set during actual read or verify of write/verify, not while trying to read headers after seeking)
2 = 1 if TIMEOUT ERROR (couldn't find header in 9 revolutions - not set while trying to read headers after seeking)
1 = N.C.
0 = 1 if operation was unsuccessful

STATUS BYTE 2

7 = 1 if SEEK ERROR - unable in 1 try to read 3 consecutive headers on a track
6 = 1 if spared sector table overflow () 32 sectors spared.
5 = N.C.
4 = 1 if bad block table overflow (greater than 100 bad blocks in table.
3 = 1 if Profile unable to read its status sector.
2 = 1 if sparing occured.
1 = 1 if seek to wrong track occurred
0 = N.C.

STATUS BYTE 3

7 = 1 if Profile has been reset.
6 = 1 if block number is invalid.
5 = 1 if block ID at end of sector mismatch*
4 = N.C.
3 = N.C.
2 = 1 if Profile was reset*
1 = 1 if Profile gave a bad response.*
0 = 1 if parity error occured*

STATUS 4

7 - 0 = the number of errors encountered when re-reading a block after any read error.

*This bits are set by the Profile driver.

FST RESULTS CHART

The Profile under test FAILS if:

1. There are 26 or more soft errors.
   a. To identify a soft error look at the Profile Status bytes.

```
S1  S2  S3  S4*   *S4 is a decimal number
08  00  00   09 <-- S4 is less than 10
```

2. There are 6 or more hard errors on the Silentype printout of the following type:

```
S1  S2  S3  S4*
08  00  00   10 <-- S4 is equal to or greater than 10.
```

3. There are 2 or more lines on the Silentype printout that are seek errors:

```
S1  S2  S3  S4*
00  02  00  00
```

4. There are ANY of the following errors or the blocks transferred counter stops counting:

   UNIT FAILS
   BUFFER COMPARE ERROR
   INVALID RANDOM SEED

   Any error with an S1 that has an odd value.
   Any error where S1 equals 04
   Any error where S1, S2 or S3 has value of FF.

5. After the Profile Final System Test as been rebooted:

   The number of SPARE SECTORS is 16 or more.
   The number of BAD BLOCKS is 1 or more.